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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	7

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No. 10/026,466	Applicant(s) NISHITOBA, SHIGEO
	Examiner Long Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with th c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-26* is/are allowed.

6)☒ Claim(s) *1-6 and 9-13* is/are rejected.

7)☒ Claim(s) *7,8,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *07 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 1/7/03 has been received and entered in the case.

Specification

2. The amendment filed on 1/7/03 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "wherein said final stage of said first current mirror circuit is arranged in a position farthest away from said reference current input terminal" on the last 2 lines of claim 1 is new and is not supported by the original disclosure.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Objections

3. Claim 9 is objected to because of the following informalities:

With respect to claim 9, the recitation "a reference ... is supplied" on lines 2-4 should be deleted because the amendment filed on 1/7/03 recites the above recitation in the independent claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 6, 9, 10, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Emeigh et al. (USP 5,767,698).

With respect to claim 1, each of Figures 4 and 5 of the Emeigh et al. reference discloses a driving circuit, which includes: a first current mirror circuit (32 in Figure 4, or 32' in Figure 5) which outputs a plurality of output currents (at the drains terminal of transistors T1-T3 in Figure 5, or at the drains terminals of transistors T1'-T3'), each of which corresponds to a reference current (reference current IREF from circuit 20); a reference input terminal (drain of transistor T0 in Figure 4, drain of T0' in Figure 5) for supplying the reference current (IREF from circuit 20) to the first current mirror circuit (32 in Figure 4, 32' in Figure 5); and a second current mirror circuit (34 in Figure 4, or 34' in Figure 5) which converts a polarity of an output current (the current at the drain terminal of transistor T3 in Figure 4, or at the drain terminal of transistor T3' in Figure 5) from a final stage (T3 in Figure 4, or T3' in Figure 5) of said first current mirror circuit (32 in Figure 4, or 32' in Figure 5) and outputs the converted output current (at the drain terminal of transistor T7 in Figure 4, or at the drain terminal of transistor T7' in Figure 5); wherein the final stage (T3 in Figure 4, or T3' in Figure 5) of the first current mirror circuit (32 in Figure 4, or 32' in Figure 5) is arranged in a position farthest away from the reference current input terminal (drain of transistor T0 in Figure 4, or drain of transistor T0' in Figure 5) as shown in the drawings of the Emeigh et al. reference.

With respect to claim 2, the Emeigh et al. reference shows that the first current mirror circuit (32 in Figure 4, 32' in Figure 5) includes: a power supply terminal (Vdd in Figure 4, GND in Figure 5) to which power is supplied (Vdd in Figure 4, GND in Figure 5); a first circuit (T0 in Figure 4, T0' in Figure 5) provided between said reference current input terminal and said power

supply terminal, to determine said plurality of output currents (drains of transistors T1-T3 in Figure 4, or drains T1'-T3' in Figure 5); a common power supply line which extends from said power supply terminal (inherently because all power supplies Vdd in the circuit are tied together, or all the grounds GND in the circuit are tied together); a plurality of output terminals (drains of transistors T1 and T2 in Figure 4, or drains of transistors T1' and T2' in Figure 5); a plurality of second circuits (T1-T2 in Figure 4, T1'-T2' in Figure 5) provided between said common power supply line (Vdd in Figure 4, GND in Figure 5) and said plurality of output terminals, to output a part of said plurality of output currents (drains of T1 and T2 in Figure 4, drains of T1' and T2' in Figure 5) determined by said first circuit (T0 in Figure 4, T0' in Figure 5) through said plurality of output terminals (drains of T1 and T2 in Figure 4, drains of T1' and T2' in Figure 5); and a third circuit (T3 in Figure 4, T3' in Figure 5) provided at a next stage of said plurality of second circuits (T1-T2 in Figure 4, T1'-T2' in Figure 5) as said final stage (T3 in Figure 4, T3' in Figure 5) of said first current mirror circuit, to output said output current (at the drain terminal of transistor T3 in Figure 4, or at the drain terminal of transistor T3' in Figure 5) determined by said first circuit (T0 in Figure 4, T0' in Figure 5).

With respect to claim 3, the second current mirror circuit (34 in Figure 4, 34' in Figure 5) converts the polarity of the output current (drain of T3 in Figure 4, or drain of T3' in Figure 5) outputted from the third circuit (T3 in Figure 4, T3' in Figure 5) and outputs said converted output current (at the drain of T7 in Figure 4, or at the drain of T7' in Figure 5) through a reference current output terminal (drain of T7 in Figure 4, or drain of T7' in Figure 5).

With respect to claim 6, Figure 5 of the Emeigh et al. reference discloses that the first circuit (T0'), the second circuits (T1'-T2') and the third circuit (T3') included in said first current

mirror circuit (32') are constituted by P-channel MOS transistors, and said second current mirror circuit (34') is constituted by N-channel MOS transistors.

With respect to claim 9, Figure 4 of the Emeigh et al. shows that the first current mirror circuit (32) includes: a ground terminal (GND) to which is connected to a ground; a first circuit (T0) provided between said reference current input terminal and said ground terminal, to determine said plurality of output currents (drains of transistors T1-T3); a common ground line which extends from the ground terminal (inherently because all the grounds GND in the circuit are tied together); a plurality of output terminals (drains of transistors T1 and T2); a plurality of second circuits (T1-T2 in Figure 4) provided between said common ground line and said plurality of output terminals, to output a part of said plurality of output currents (drains of T1 and T2) determined by said first circuit (T0) through said plurality of output terminals (drains of T1 and T2); and a third circuit (T3) provided at a next stage of said plurality of second circuits (T1-T2) as said final stage (T3) of said first current mirror circuit (32), to output said output current (at the drain terminal of transistor T3) determined by said first circuit (T0).

With respect to claim 10, Figure 4 of the Emeigh et al. reference shows that the second current mirror circuit (34) converts the polarity of the output current (drain of T3) outputted from the third circuit (T3) and outputs said converted output current (at the drain of T7) through a reference current output terminal (drain of T7).

With respect to claim 13, Figure 4 of the Emeigh et al. reference shows that the first circuit (T0), said second circuits (T1, T2) and the third circuit (T3) included in said first current mirror circuit (32) are constituted by N-channel MOS transistors, and said second current mirror circuit (34) is constituted by P-channel MOS transistors.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emeigh et al. (USP 5,767,698) in view of Nayebi et al. (USP 6,384,638).

With respect to claim 4, Figure 5 of the Emeigh et al. reference discloses a driving circuit as discussed above with regard to the 102(b) rejection which includes all the limitations of this claim except the circuit is fabricated using bipolar technology. However, the Nayebi et al. reference teaches that using bipolar technology to fabricate a circuit is less expensive than using BiCMOS technology (see Col. 4, lines 5-6 of the Nayebi et al. reference). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the Emeigh et al. reference to fabricate the driving circuit in Figure 5 of the Emeigh et al. reference using bipolar technology as taught by the Nayebi et al. reference instead of BiCMOS technology, e.g., each of the N-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by an NPN transistor and each of the P-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by a PNP transistor, for the purpose saving cost. Thus, this modification meets all the limitations of claim 4 because the first circuit (T0'), the second circuits (T1' and T2') and the third circuit (T3') included in the first current mirror circuit (32') are constituted by PNP transistors (because each of the P-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by a PNP transistor as discussed in the modification), and the second mirror

circuit (34') is constituted by NPN transistors (because each of the N-channel transistors in Figure 5 of the Emeigh et al. reference is replaced by an NPN transistor as discussed in the modification).

With respect to claim 11, Figure 4 of the Emeigh et al. reference discloses a driving circuit as discussed above with regard to the 102(b) rejection which includes all the limitations of this claim except the circuit is fabricated using bipolar technology. However, the Nayebi et al. reference teaches that using bipolar technology to fabricate a circuit is less expensive than using BiCMOS technology (see Col. 4, lines 5-6 of the Nayebi et al. reference). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the Emeigh et al. reference to fabricate the driving circuit in Figure 4 of the Emeigh et al. reference using bipolar technology as taught by the Nayebi et al. reference instead of BiCMOS technology, e.g., each of the N-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by an NPN transistor and each of the P-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by a PNP transistor, for the purpose saving cost. Thus, this modification meets all the limitations of claim 11 because the first circuit (T0), the second circuits (T1 and T2) and the third circuit (T3) included in the first current mirror circuit (32) are constituted by NPN transistors (because each of the N-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by an NPN transistor as discussed in the modification), and the second mirror circuit (34) is constituted by PNP transistors (because each of the P-channel transistors in Figure 4 of the Emeigh et al. reference is replaced by a PNP transistor as discussed in the modification).

8. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emeigh et al. (USP 5,767,698) in view of Nayebi et al. (USP 6,384,638), and further in view of Kipnis (USP 6,326,836).

With respect to claim 5, the driving circuit as discussed in the above modification (Figure 5 of Emeigh et al. in view of Nayebi et al.) with regard to the rejection of claim 4 meets all the limitations of this claim except for the limitation that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits (32' and 34') in the above modification (Figure 5 of Emeigh et al. in view of Nayebi et al.) with a base current compensation circuit as taught by the Kipnis reference for the purpose of preventing excessive loading of the base connections of the transistors in each of the current mirror circuits. Thus, this modification meets all the limitations of claim 5.

With respect to claim 12, the driving circuit as discussed in the above modification (Figure 4 of Emeigh et al. in view of Nayebi et al.) with regard to the rejection of claim 11 meets all the limitations of this claim except for the limitation that at least one of the first current mirror

circuit and the second current mirror circuit has a base current compensation circuit. However, the Kipnis reference discloses that each of the current mirror circuits in Figure 2 includes a current compensation circuit (i.e., current mirror circuit 203, 205 and 207 including a current compensation circuit 205; current mirror circuit 209, 211 and 213 including a current compensation circuit 211; and current mirror circuit 215, 217 and 219 including a current compensation circuit 217) for the purpose of preventing excessive loading of the base connections of the transistors in the current mirror circuit (Col. 1, lines 36-62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the first and second current mirror circuits (32 and 34) in the above modification (Figure 4 of Emeigh et al. in view of Nayebi et al.) with a base current compensation circuit as taught by the Kipnis reference for the purpose of preventing excessive loading of the base connections of the transistors in each of the current mirror circuits. Thus, this modification meets all the limitations of claim 12.

Allowable Subject Matter

9. Claims 16-26 are allowed.

Claim 16 is allowed because the prior art of record does not disclose or suggest a constant driving apparatus comprising a plurality of driving circuits connected through terminals in series, wherein each of the driving circuits includes a first current mirror circuit which outputs a plurality of plurality of output currents, each of which corresponds to a reference current, and a second current mirror circuit which converts a polarity of an output current outputted from a final stage of the first current mirror circuit and outputs the converted output current.

Claims 17-26 are allowed because they depend on claim 16.

10. Claims 7, 8, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the power supply terminal is pulled out from a center of the common power supply line.

Claim 8 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the power supply terminal is pulled out from a plurality of positions of the common power supply line.

Claim 14 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the ground terminal is pulled out from a center of the common ground line.

Claim 15 would be allowed because the prior art of record does not disclose or suggest that at least one of the first current mirror circuit and the second current mirror circuit has a base current compensating circuit and wherein the ground terminal is pulled out from a plurality of positions of the common ground supply line.

Response to Arguments

11. Applicant's arguments with respect to claim 1 filed on 1/7/03 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

3/18/03
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Long Nguyen
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Primary Examiner